AMENDMENTS TO THE CLAIMS:

1. (Cancelled)

2. (Previously Presented) A delay locked loop comprising:

a delay circuit for delaying a first clock to output a second clock;

a detector for detecting which of said first and second clocks is advanced in a phase; and

a gray code counter using a gray code, responsive to an output of said detector, for selectively generating one of a signal to increase an amount of delay of said delay circuit and a signal to decrease said amount of delay of said delay circuit;

wherein said output of said detector indicates that said first clock is in advance of said second clock in a phase or said second clock is in advance of said first clock in a phase;

wherein said gray code counter includes:

a gray code register for storing said gray code;

a binary code converter for converting said gray code into a binary code;

an upward carry/downward carry generator using said binary code stored in said binary code converter, to generate an upward carry signal and a downward carry signal; and

a carry multiplexer generating from said upward carry signal and said downward carry signal a carry signal corresponding to a result obtained by said detector, for updating said gray code in said gray code register.

3. (Original) The delay locked loop according to claim 2, wherein said delay circuit includes a fine delay element and a coarse delay element having an amount of delay greater per unit than said fine delay element, said fine delay element having an amount of delay adjusted by said

binary code stored in said binary code converter, said coarse delay element having an amount of delay adjusted by said gray code stored in said gray code register.

4. (Cancelled)

5. (Previously Presented) A semiconductor device comprising a delay locked loop including:

an input buffer for receiving an external clock and outputting a first internal clock;

a delay circuit for delaying said first internal clock to output a second internal clock;

a detector for detecting which of said first and second clocks is advanced in a phase; and

a gray code counter using a gray code, responsive to an output of said detector, for selectively generating one of a signal to increase an amount of delay of said delay circuit and a signal to decrease said amount of delay of said delay circuit;

wherein said output of said detector indicates that said first clock is in advance of said second clock in a phase or said second clock is in advance of said first clock in a phase;

wherein said gray code counter includes:

a gray code register for storing said gray code;

a binary code converter for converting said gray code into a binary code;

an upward carry/downward carry generator using said binary code stored in said binary code converter, to generate an upward carry signal and a downward carry signal; and

a carry multiplexer generating from said upward carry signal and said downward carry signal a carry signal corresponding to a result obtained by said detector, for updating said gray code in said gray code register.

6. (Previously Presented) The semiconductor device according to claim 5, wherein said delay circuit includes a fine delay element and a coarse delay element having an amount of delay greater per unit than said fine delay element, said fine delay element having an amount of delay adjusted by said binary code stored in said binary code converter, said coarse delay element having an amount of delay adjusted by said gray code stored in said gray code register.

7. (Original) The semiconductor device according to claim 5, further comprising an input circuit operative in response to said second internal clock to externally receive a signal.

8. (Original) The semiconductor device according to claim 7, further comprising a memory cell array including a plurality of memory cells, wherein said input circuit receives a signal for writing/reading data to/from said memory cell array.

9. (Original) The semiconductor device according to claim 5, further comprising an output circuit operative in response to said second internal clock to externally output a signal.

10. (Original) The semiconductor device according to claim 9, further comprising a memory cell array including a plurality of memory cells, wherein said output circuit externally outputs data read from said memory cell array.

11. (Previously Presented) A semiconductor device comprising a delay locked loop including:

a first input buffer for receiving at least a first external clock and a second external clock complementary in phase to said first external clock, and outputting a first internal clock at the timing of the rising edge of said first external clock when a potential of said first external clock is equal to that of said second external clock;

a second input buffer for receiving at least said first and second external clocks, and outputting a second internal clock at the timing of the rising edge of said second external clock when a potential of said first external clock is equal to that of said second external clock;

a first delay circuit for delaying said first internal clock to output a third internal clock;

a second delay circuit for delaying said second internal clock to output a fourth internal clock;

a detector for detecting which of said first and second clocks is advanced in a phase; and

a gray code counter using a gray code, responsive to an output of said detector for selectively generating one of a signal to increase an amount of delay of said first delay circuit and an amount of delay of said second delay circuit, and a signal to decrease said amount of delay of said first delay circuit and said amount of delay of said second delay circuit;

wherein said output of said detector indicates that said first clock is in advance of said second clock in a phase or said second clock is in advance of said first clock in a phase.

12. (Original) The semiconductor device according to claim 11, further comprising an output circuit operative in response to said third and fourth internal clocks to externally output a signal.

13. (Original) The semiconductor device according to claim 12 further comprising a memory cell array including a plurality of memory cells, wherein said output circuit is responsive to said third and fourth internal clocks for externally outputting data read from said memory cell array.

14. (Cancelled)

15. (Previously Presented) A control method for a system operating in synchronization with a clock, comprising the steps of:

inputting an external clock to an input buffer to generate a first internal clock therefrom;

delaying said first internal clock to output a second internal clock;

detecting which of said first and second clocks is advanced in a phase; and

using a gray code, responsive to a result obtained in the step of detecting, to selectively generate one of a signal to increase an amount of delay to be applied in the step of delaying and a signal to decrease said amount of delay to be applied in the step of delaying;

wherein said result of detecting indicates that said first clock is in advance of said second clock in a phase or said second clock is in advance of said first clock in a phase;

wherein the step of using the gray code includes the steps of:

converting said gray code into a binary code;

using said binary code to produce an upward carry signal and a downward carry signal; and

referring to a result obtained in the step of detecting, to generate a carry signal from said upward carry signal and said downward carry signal for updating said gray code.

16. (Original) The method according to claim 15, further comprising the step of externally outputting data in response to said second internal clock.

17. (Original) The method according to claim 15, further comprising the step of externally receiving data in response to said second internal clock.